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PEARNE & GORDON LLP
1801 EAST 9TH STREET
SUITE 1200
CLEVELAND, OH 44114-3108

EXAMINER	
TRAN, THIEN S	
ART UNIT	PAPER NUMBER
3742	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patdocket@pearne.com
dchervenak@pearne.com

Office Action Summary	Application No.	Applicant(s)	
	10/599,431	SUENAGA ET AL.	
	Examiner	Art Unit	
	THIEN TRAN	3742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13,14 and 16-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 13, 14 and 16-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 13 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) and (JP 62-66595). An English-language translation of the Abstract has been provided for JP 62-66595 and is included in PTO-892 Notice of Reference Cited.

4. Regarding claim 1, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40);

a series circuit including two semiconductor switching devices (Fig 1, Items 36 & 37, Col 7, Lines 60-63), the series circuit being connected in parallel to the DC power supply (Fig 1, Items 36 & 37 are connected in parallel to Item 31); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), one end of the resonance circuit being connected to a middle point of the series circuit (Fig 1, Item 34 is connected between Items 36 and 37) while the other end of the resonance circuit is connected to one end of the DC power supply (Fig 1, Item 34 is connected to positive terminal of Item 31); a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently (Fig 4a & 4c, Items 36 & 37). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

5. Bessyo discloses the claimed invention except for a frequency-modulated signal generation unit operable to transmit a frequency-modulated signal; a lowest frequency limiting unit for establishing a lowermost limit of a frequency at which the semiconductor switching devices are to be operated, the lowest limit frequency limiting

unit establishes the lowermost limit as a first frequency when the high-frequency heating apparatus is activated and gradually lowers the lowermost limit to a second frequency that is less than the first frequency in response to activation of the high-frequency heating apparatus; a comparison unit for comparing the frequency-modulated signal to the lowermost limit as the lowermost limit is being gradually lowered by the lowest frequency limiting unit, the comparison unit transmits a comparison result signal indicating which of the frequency-modulated signal and the lowermost limit is greater, the comparison result signal to be communicated to the drive unit for controlling operation of the semiconductor switching devices; the drive unit is operable to drive the semiconductor switching devices based on the comparison result signal transmitted by the comparison unit.

6. In analogous art of method of controlling inverter power source for magnetron, JP 62-66595 discloses a frequency-modulated signal generation unit (Fig 1, Item 10d, Frequency conversion circuit, Abstract, Lines 5-7) operable to transmit a frequency-modulated signal; a lowest frequency limiting unit (Fig 1, Item 10B, Reference circuit, Abstract, Lines 3-4) for establishing a lowermost limit of a frequency at which the semiconductor switching devices (Fig 1, Item 6, Power switching element) are to be operated, the lowest limit frequency limiting unit establishes the lowermost limit as a first frequency when the high-frequency heating apparatus is activated and gradually lowers the lowermost limit to a second frequency that is less than the first frequency in response to activation of the high-frequency heating apparatus; a comparison unit (Fig 1, Item 10C, Comparing circuit, Abstract, Lines 4-5) for comparing the frequency-

modulated signal to the lowermost limit as the lowermost limit is being gradually lowered by the lowest frequency limiting unit, the comparison unit transmits a comparison result signal indicating which of the frequency-modulated signal and the lowermost limit is greater, the comparison result signal to be communicated to the drive unit (Fig 1, Item 10F, Driving circuit, Abstract, Line 9) for controlling operation of the semiconductor switching devices; the drive unit (Fig 1, Item 10F, Driving circuit, Abstract, Line 9) is operable to drive the semiconductor switching devices based on the comparison result signal transmitted by the comparison unit for purpose of forming a control device which includes an inverter power source which drives a magnetron by a high frequency voltage by an inverter (Abstract, Lines 1-2). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the circuit structure of JP 62-66595 for the purpose of forming a control device which includes an inverter power source which drives a magnetron by a high frequency voltage by an inverter.

7. Regarding claim 3, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10) a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a series circuit including two semiconductor switching devices (Fig 1, Items 36 & 37, Col 7, Lines 60-63), the series circuit being connected in parallel to the DC power

supply (Fig 1, Items 36 & 37 are connected in parallel to Item 31); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), the resonance circuit being connected in parallel to one of the semiconductor switching devices (Items 34 & 35 are connected in parallel to Item 37); a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently (Fig 4a & 4c, Items 36 & 37). Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

8. Bessyo discloses the claimed invention except for a frequency-modulated signal generation unit operable to transmit a frequency-modulated signal; a lowest frequency limiting unit for establishing a lowermost limit of a frequency at which the semiconductor switching devices are to be operated, the lowest limit frequency limiting unit establishes the lowermost limit as a first frequency when the high-frequency heating apparatus is activated and gradually lowers the lowermost limit to a second frequency that is less than the first frequency in response to activation of the high-frequency heating apparatus; a comparison unit for comparing the frequency-

modulated signal to the lowermost limit as the lowermost limit is being gradually lowered by the lowest frequency limiting unit, the comparison unit transmits a comparison result signal indicating which of the frequency-modulated signal and the lowermost limit is greater, the comparison result signal to be communicated to the drive unit for controlling operation of the semiconductor switching devices; the drive unit is operable to drive the semiconductor switching devices based on the comparison result signal transmitted by the comparison unit.

9. In analogous art of method of controlling inverter power source for magnetron, JP 62-66595 discloses a frequency-modulated signal generation unit (Fig 1, Item 10d, Frequency conversion circuit, Abstract, Lines 5-7) operable to transmit a frequency-modulated signal; a lowest frequency limiting unit (Fig 1, Item 10B, Reference circuit, Abstract, Lines 3-4) for establishing a lowermost limit of a frequency at which the semiconductor switching devices (Fig 1, Item 6, Power switching element) are to be operated, the lowest limit frequency limiting unit establishes the lowermost limit as a first frequency when the high-frequency heating apparatus is activated and gradually lowers the lowermost limit to a second frequency that is less than the first frequency in response to activation of the high-frequency heating apparatus; a comparison unit (Fig 1, Item 10C, Comparing circuit, Abstract, Lines 4-5) for comparing the frequency-modulated signal to the lowermost limit as the lowermost limit is being gradually lowered by the lowest frequency limiting unit, the comparison unit transmits a comparison result signal indicating which of the frequency-modulated signal and the lowermost limit is greater, the comparison result signal to be communicated to the drive

unit (Fig 1, Item 10F, Driving circuit, Abstract, Line 9) for controlling operation of the semiconductor switching devices; the drive unit (Fig 1, Item 10F, Driving circuit, Abstract, Line 9) is operable to drive the semiconductor switching devices based on the comparison result signal transmitted by the comparison unit for purpose of forming a control device which includes an inverter power source which drives a magnetron by a high frequency voltage by an inverter (Abstract, Lines 1-2). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the circuit structure of JP 62-66595 for the purpose of forming a control device which includes an inverter power source which drives a magnetron by a high frequency voltage by an inverter.

10. Regarding claims 13 and 30, as applied to claims 1 and 3, Bessyo teaches the dead time generation circuit (Fig 1, Items 34-37) generates a dead time based on positive and negative offset voltages (Fig 4b & 4d, Items 3 & 37) each varying with a first inclination in proportion to increase of a switching frequency and varying with a second inclination when the switching frequency reaches a predetermined frequency or higher.

11. Claims 2 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) in view of Manabu (Japan Patent Publication 2003-259643) and (JP 62-66595). An English-language equivalent has been adopted for Japanese reference Manabu (Japan Patent Publication 2003-259643) and is included in PTO-892 Notice of Reference Cited.

12. Regarding claim 2, Bessyo teaches a high-frequency heating apparatus for driving a magnetron (Col 5, Lines 66-67), comprising: a DC power supply (Fig 1, Item 31, Col 7, Line 57) including an AC power supply (Fig 7, AC Source, Col 11, Lines 7-10), a rectifier circuit (Fig 1, Item 40, Col 7, Line 56) for rectifying a voltage of the AC power supply, and a smoothing capacitor (Fig 1, Item 43, Col 9, Lines 55-56) for smoothing an output voltage of the rectifier circuit (Fig 1, Item 35, Col 11, Lines 35-40); a resonance circuit (Fig 1, Items 34 & 35, Col 9, Lines 5-20) connected to a primary winding (Fig 1, Item 33, Col 7, Line 60) of a leakage transformer and a capacitor (Fig 1, Item 32, Col 7, Line 60), a drive unit (Fig 1, Item 38, Col 8, Line 20) for driving each of the semiconductor switching devices; a rectifier unit (Fig 1, Item 40, Col 7, Line 56) connected to a secondary winding (Fig 1, Item 39, Col 8, Line 1) of the leakage transformer; a magnetron (Fig 1, Item 41, Col 7, Line 57) connected to the rectifier unit (Fig 1, Item 41 is connected to Item 40); and a dead time generation circuit (Fig 1, Items 34-37) for turning off the semiconductor switching devices concurrently. Examiner interprets that Bessyo teaches a variable dead time preparation circuit because in Fig 4a & 4c, in modes 2 & 5, the first (Item 36) and second (Item 37) switching devices are simultaneously turned off (Current = 0) in response to the switching frequency.

13. Bessyo discloses the claimed invention except for two series circuits each including two semiconductor switching devices, each of the series circuits being connected in parallel to the DC power supply; one end of the resonance circuit being connected to a middle point of one of the series circuits while the other end of the

resonance circuit is connected to a middle point of the other series circuit; a frequency-modulated signal generation unit operable to transmit a frequency-modulated signal; a lowest frequency limiting unit for establishing a lowermost limit of a frequency at which the semiconductor switching devices are to be operated, the lowest limit frequency limiting unit establishes the lowermost limit as a first frequency when the high-frequency heating apparatus is activated and gradually lowers the lowermost limit to a second frequency that is less than the first frequency in response to activation of the high-frequency heating apparatus; a comparison unit for comparing the frequency-modulated signal to the lowermost limit as the lowermost limit is being gradually lowered by the lowest frequency limiting unit, the comparison unit transmits a comparison result signal indicating which of the frequency-modulated signal and the lowermost limit is greater, the comparison result signal to be communicated to the drive unit for controlling operation of the semiconductor switching devices; the drive unit is operable to drive the semiconductor switching devices based on the comparison result signal transmitted by the comparison unit.

14. In analogous art of current resonance type soft switching power circuit, Manabu discloses two series circuits including two semiconductor switching devices (Drawing 1, Q1 & Q2 is the first series circuit, Q3 & Q4 is the second series circuit, Pg 20, Description of Notations), each of the series circuits being connected in parallel to the DC power supply (Drawing 1, First Series (Q1 & Q2) and Second Series (Q3 & Q4) are in parallel with Item E, Pg 20, Description of Notations); one end of the resonance circuit being connected to a middle point of one of the series circuits (Drawing 1, Item

2, Rectification Circuit is connected between Q1 & Q2) while the other end of the resonance circuit is connected to a middle point of the other series circuit (Drawing 1, Item 2, Rectification Circuit is connected between Q2 & Q3) for the benefit of providing soft switching in a current resonance type soft switching power circuit (Abstract, Pg 2, Lines 1-3). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Manabu for the benefit of providing soft switching in a current resonance type soft switching power circuit.

15. In analogous art of method of controlling inverter power source for magnetron, JP 62-66595 discloses a frequency-modulated signal generation unit (Fig 1, Item 10d, Frequency conversion circuit, Abstract, Lines 5-7) operable to transmit a frequency-modulated signal; a lowest frequency limiting unit (Fig 1, Item 10B, Reference circuit, Abstract, Lines 3-4) for establishing a lowermost limit of a frequency at which the semiconductor switching devices (Fig 1, Item 6, Power switching element) are to be operated, the lowest limit frequency limiting unit establishes the lowermost limit as a first frequency when the high-frequency heating apparatus is activated and gradually lowers the lowermost limit to a second frequency that is less than the first frequency in response to activation of the high-frequency heating apparatus; a comparison unit (Fig 1, Item 10C, Comparing circuit, Abstract, Lines 4-5) for comparing the frequency-modulated signal to the lowermost limit as the lowermost limit is being gradually lowered by the lowest frequency limiting unit, the comparison unit transmits a comparison result signal indicating which of the frequency-modulated signal and the

lowermost limit is greater, the comparison result signal to be communicated to the drive unit (Fig 1, Item 10F, Driving circuit, Abstract, Line 9) for controlling operation of the semiconductor switching devices; the drive unit (Fig 1, Item 10F, Driving circuit, Abstract, Line 9) is operable to drive the semiconductor switching devices based on the comparison result signal transmitted by the comparison unit for purpose of forming a control device which includes an inverter power source which drives a magnetron by a high frequency voltage by an inverter (Abstract, Lines 1-2). It would have been obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and Manabu with the circuit structure of JP 62-66595 for the purpose of forming a control device which includes an inverter power source which drives a magnetron by a high frequency voltage by an inverter.

16. Regarding claim 22, as applied to claim 2, Bessyo teaches the dead time generation circuit (Fig 1, Items 34-37) generates a dead time based on positive and negative offset voltages (Fig 4b & 4d, Items 3 & 37) each varying with a first inclination in proportion to increase of a switching frequency and varying with a second inclination when the switching frequency reaches a predetermined frequency or higher.

17. Claims 4, 5, 6, 24, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) and (JP 62-66595) as applied to claims 1 and 3, in view of Noda (US Patent 5,274,208).

18. Regarding claims 4 and 24, Bessyo and JP 6266595 discloses the claimed invention except for an error signal generation circuit for generating an error signal from a difference between an input current of the AC power supply and a reference

current; and a frequency-modulated signal generation unit corrects a rectified voltage/rectified current obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit being supplied to the dead time generation circuit; the lowest frequency limiting unit is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit.

19. In analogous art of high frequency heating apparatus, Noda discloses an error signal generation circuit (Fig 2, Item 26, Col 6, Line 44) for generating an error signal from a difference between an input current of the AC power supply and a reference current (Col 6, Lines 39-44); and a frequency-modulated signal generation unit (Fig 2, Item 27, Col 6, Lines 45-49) corrects a rectified voltage/rectified current (Fig 2, Item 25, Col 6, Lines 39-42) obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit (Fig 2, Item S3, Col 6, Lines 50-54) being supplied to the dead time generation circuit; the lowest frequency limiting unit (Fig 2, Item 34, Col 7, Lines 13-15) is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and JP 62-66595 with the disclosure of Noda for the benefit of providing a

magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied.

20. Regarding claim 5, as applied to claims 1 and 4, Bessyo and JP 62-66595 discloses the claimed invention except for the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged.

21. In analogous art of high frequency heating apparatus, Noda discloses the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and JP 62-66595 with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is known in the art that the

overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

22. Regarding claim 6, as applied to claim 1 and 4, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being well known in the art (Specification, Pg 29, Lines 1-2).

23. Regarding claim 25, as applied to claims 3 and 24, Bessyo and JP 62-66595 discloses the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and JP 62-66595 with the disclosure of Noda for the benefit of providing a magnetron that can be

driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is well known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

24. Regarding claim 26, as applied to claims 3 and 24, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being well known in the art (Specification, Pg 29, Lines 1-2).

25. Claims 7, 9, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) and (JP 62-66595) as applied to claims 1 and 3, in view of Teruya (Japan Patent Publication 2003-257604). An English-language equivalent has been adopted for Japanese reference Teruya (Japan Patent Publication 2003-257604) and is included in PTO-892 Notice of Reference Cited.

26. Regarding claims 7 and 27, Bessyo and JP 62-66595 discloses the claimed invention except for the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been

obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and JP 62-66595 with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

27. Regarding claim 9, as applied to claims 1 and 7, Bessyo and JP 62-66595 disclosed the claimed invention except for the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and JP 62-66595 with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

28. Regarding claim 29, Bessyo and JP 62-66595 discloses the claimed invention except for the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg

13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and JP 62-66595 with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

29. Claims 8 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463), (JP 62-66595) and Teruya (Japan Patent Publication 2003-257604) as applied to claims 1, 3 and 7, in view of Manabu (Japan Patent Publication 2003-259643).

30. Regarding claim 8, Bessyo, JP 62-66595 and Teruya discloses the claimed invention except for the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, JP 62-66595 and Teruya with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

31. Regarding claim 28, as applied to claims 3 and 27, Bessyo, JP 62-66595 and Teruya discloses the claimed invention except for the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current resonance type soft switching power circuit, Manabu discloses the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, JP 62-66595 and Teruya with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

32. Claims 14 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463) and (JP 62-66595) as applied to claims 1 and 3, in view of Yang (US Patent Publication 2005/0174819).

33. Regarding claims 14 and 31, Bessyo teaches the dead time generation circuit includes a first current varying in proportion to a switching frequency (Fig 4, Item a), a second current beginning flowing at a predetermined frequency at beginning (Fig 13, Col 13, Lines 50-59) and varying in proportion to the switching frequency (Fig 3, Item c). Bessyo and JP 62-66595 discloses the claimed invention except for the dead time generation circuit includes a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient, and a upper and lower

potential generation unit for generating a set of upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the set of upper and lower potentials.

34. In analogous art of synchronous rectification circuit with dead time regulation, Yang discloses where the dead time generation circuit includes a VCC power supply (Pg 2, 0022), a duty control power supply (Pg 2, 0022), a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient and a upper and lower potential generation unit for generating a set of upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the set of upper and lower potentials (Pg 1, 0014) for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform (Pg 1, 0012). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo and JP 62-66595 with the disclosure of Yang for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform.

35. Claims 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463), Manabu (JP 2003-259643) and JP 62-66595 as applied to claim 2, in view of Noda (US Patent 5,274,208).

36. Regarding claim 16, Bessyo, Manabu and JP 62-66595 discloses the claimed invention except for an error signal generation circuit for generating an error signal

from a difference between an input current of the AC power supply and a reference current; and the frequency-modulated signal generation unit corrects a rectified voltage/rectified current obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit being supplied to the dead time generation circuit; the lowest frequency limiting circuit is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit.

37. In analogous art of high frequency heating apparatus, Noda discloses an error signal generation circuit (Fig 2, Item 26, Col 6, Line 44) for generating an error signal from a difference between an input current of the AC power supply and a reference current (Col 6, Lines 39-44); the frequency-modulated signal generation unit (Fig 2, Item 27, Col 6, Lines 45-49) corrects a rectified voltage/rectified current (Fig 2, Item 25, Col 6, Lines 39-42) obtained by rectifying the AC power supply, based on an output (error signal) of the error signal generation circuit, an output of the frequency-modulated signal generation circuit (Fig 2, Item S3, Col 6, Lines 50-54) being supplied to the dead time generation circuit; the lowest frequency limiting unit (Fig 2, Item 34, Col 7, Lines 13-15) is inserted between the frequency-modulated signal generation circuit and the dead time generation circuit for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Manabu and JP 62-66595 with the disclosure of Noda for the benefit of

providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied.

38. Regarding claim 17, Bessyo, Manabu and JP 62-66595 discloses the claimed invention except for the lowest frequency limiting circuit has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied to the dead time generation circuit, and charges accumulated in the capacitor are discharged. In analogous art of high frequency heating apparatus, Noda discloses the lowest frequency limiting circuit (Fig 2, Item 34, Col 7, Lines 13-15) has a capacitor, the capacitor is charged during suspension of the high-frequency heating apparatus, and as soon as the high-frequency heating apparatus begins to operate, a voltage of the capacitor is supplied (Fig 2, Item Vmax, Col 7, Lines 10-15), to the dead time generation circuit and charges accumulated in the capacitor are discharged (Fig 2, Item S5, Col 7, Lines 12-18) for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied (Col 1, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Manabu and JP 62-66595 with the disclosure of Noda for the benefit of providing a magnetron that can be driven normally in its operation range even when different commercial power supply voltages are supplied. Examiner interprets that it is known in the art that the overvoltage detection circuit of Noda has a capacitor for generating signal S5 (Fig 2, Item S5, Col 7, Lines 12-18).

39. Regarding claim 18, the applicant discloses that the dead time generation circuit generates a fixed or marginally increased dead time regardless of a switching frequency as being known in the art (Specification, Pg 29, Lines 1-2).

40. Claims 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US Patent 6,362,463), Manabu (JP 2003-259643) and JP 62-66595 as applied to claim 2, in view of Teruya (Japan Patent Publication 2003-257604).

41. Regarding claim 19, Bessyo, Manabu and JP 62-66595 discloses the claimed invention except for the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit generates a dead time increased in accordance with increase of a switching frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Manabu and JP 62-66595 with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

42. Regarding claim 20, Bessyo discloses the claimed invention except for the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency. In analogous art of current

resonance type soft switching power circuit, Manabu discloses the dead time generation circuit fixes or marginally increases the dead time at a switching frequency not higher than a predetermined frequency (Pg 13, 0028, Lines 15-17) for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output (Pg 13, 0028, Lines 16-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo with the disclosure of Manabu for the benefit of providing operational stability of a circuit, changing a cycle, and performing an output.

43. Regarding claim 21, Bessyo, Manabu and JP 62-66595 discloses the claimed invention except for the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency. In analogous art of inverter cooker, Teruya discloses the dead time generation circuit suddenly increases the dead time at a switching frequency not lower than a predetermined frequency (Pg 13, 0035, dead time is enlarged, Drawing 4c & 4d) for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current (Abstract, Pg 2, Lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Manabu and JP 62-66595 with the disclosure of Teruya for the benefit of allowing input to be continuously variable from high to low without causing excessive rise in driving frequency or passage of a short circuit current.

44. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US 6,362,463), Manabu (JP 2003-259643) and JP 62-66595 as applied to claim 2, in view of Yang (US 2005/0174819).

45. Regarding claim 23, Bessyo teaches the dead time generation circuit includes a first current varying in proportion to a switching frequency (Fig 4, Item a), a second current beginning to flow at a predetermined frequency and varying in proportion to the switching frequency (Fig 3, Item c). Bessyo, Manabu and JP 62-66595 discloses the claimed invention except for the dead time generation circuit includes a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient, and a upper and lower potential generation unit for generating two upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials.

46. In analogous art of synchronous rectification circuit with dead time regulation, Yang discloses where the dead time generation circuit includes a VCC power supply (Pg 2, 0022), a duty control power supply (Pg 2, 0022), a third current obtaining by and multiplying a combining current of the two currents by a predetermined coefficient and a upper and lower potential generation unit for generating two upper and lower potentials obtained by adding positive and negative offset voltages proportional to the third current, to the duty control power supply respectively, and a dead time is generated based on the two upper and lower potentials (Pg 1, 0014) for the benefit of

improving the long dead time and efficiency resulting from an unstable voltage waveform (Pg 1, 0012). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Bessyo, Manabu and JP 62-66595 with the disclosure of Yang for the benefit of improving the long dead time and efficiency resulting from an unstable voltage waveform.

Response to Amendment

42. Claims 1, 2, 3, 4, 16, and 24 have been amended.

43. Claims 10-12 and 15 are cancelled.

44. Claims 1-9, 13, 14 and 16-31 are pending.

Response to Arguments

45. Applicant's arguments with respect to claims 1-3 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIEN TRAN whose telephone number is (571)270-7745. The examiner can normally be reached on Mon-Friday, 8-5PM EST.

47. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tu Hoang can be reached on 571-272-4780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/THIEN TRAN/
Examiner, Art Unit 3742
7/13/2011

/Henry Yuen/
Supervisory Patent Examiner,
TC 3700